Improved Architecture of FDTD Dataflow Machine for Larger Scale Microwave Simulation

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As a portable High Performance Computing (HPC) technology for microwave simulations, several kinds of dedicated computers for the Finite-Difference Time-Domain (FDTD) method have been considered. Author also proposed a dataflow architecture FDTD dedicated computer and it was shown that the estimated performance of the FDTD dataflow machine can exceed those of the high-end PC and GPU computers. On the other hand, the digital circuit of the FDTD dataflow machine was inefficiently implemented on the Field-Programmable Gate Array (FPGA) owing to dual operation modes of a normal FDTD grid and Perfectly Matched Layer (PML) grid, that is, almost half part of FPGA was not used in the conventional machine. This paper proposes an improved architecture of the 3-D FDTD dedicated computer with the dual operation modes to improve the efficiency in its implementation on the FPGA.

***Index Terms*—High performance computing, Microwave simulation, Finite-difference time domain (FDTD) method, Dedicated computer, Dataflow architecture, Field programmable gate array (FPGA)**

I. Introduction

In the last decade, applications of microwave simulations have been spreading out rapidly owing to downsizing of HPC technologies such as a high-end PC. Several kinds of commercial software based on the FDTD method were also provided and used in industry applications widely. On the other hand, the computer performance is not sufficient yet for large scale FDTD simulations even in use of the highest-end computers, typically, several thousand time steps FDTD calculation for 500 x 500 x 500 grid space takes about 24 hours. In particular, the FDTD method is a heavy memory access scheme, and therefore, parallel processing such as the MPI cannot effectively speed up the microwave simulations due to heavy data communication between computer nodes. On the other hand, it is also known that the GPU computers can speed-up the FDTD scheme calculation at most by ten times higher compared with the high-end PC owing to the heavy memory access between the GPU and the main memory. Accordingly, we need to introduce any other types of computer systems to achieve potentially much higher speed FDTD microwave simulations than those of conventional Neumann's architecture machines for practical uses in industry applications. From this point of view, various kinds of the FDTD method dedicated computers have been developed [1]-[5]. The author has been also working in the development of the dedicated computer, and a basic concept and its detail circuit design of a dataflow architecture FDTD machine were proposed as a extremely HPC system [5]. It was shown that the FDTD dataflow machine has 50 times higher performance than those of GPU computers at least. However, owing to dual mode operation of a normal and PML grids circuit, the FDTD dataflow machine was implemented on the FPGA inefficiently. This paper presents modified circuit design of the FDTD dataflow machine to be efficient implementation on the FPGA for larger scale simulations.

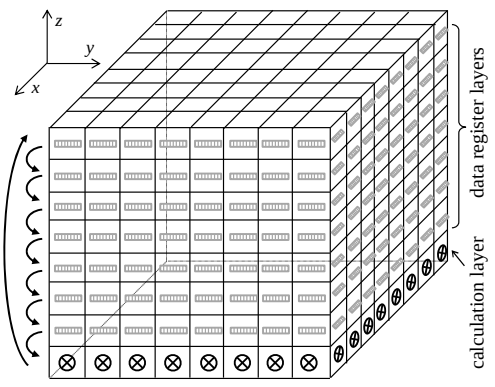

Fig. 1. Configuration of dataflow architecture FDTD machine

II. Configuration of FDTD Dataflow Machine

A conceptual configuration of the dataflow architecture of 3-D FDTD method dedicated computer is indicated in Fig.1 [5]. All the values of electromagnetic field components are stored in data registers which are logically allocated as 3-D grid structure, and are connected to vertically neighbor grids. The dedicated digital circuits of the FDTD scheme are allocated only in the lowest horizontal (*x*-*y*) plane. That is, the FDTD calculations for three electric/magnetic field components in all grids of the lowest horizontal *x*-*y* layer are executed simultaneously in a single clock, and after that upper layer field values are shifted down by rotational rule for vertical (*z*) direction. Accordingly, a single time step FDTD calculation of the electric and magnetic fields for entire 3-D grid space is executed in 4 x N_z clock cycles including the vertical shift, if we assume that the number of grid size for *z*-direction is N_z. For example, the estimated performance of the dataflow architecture FDTD machine reaches to 125G cells/sec if the *x*-*y* plane is 100 x 100 grids size.

A circuit of *z*-component of electric field in a unit grid of the dataflow architecture of the conventional FDTD dedicated computer is indicated in Fig.2. In the dedicated circuit, the PML scheme is also invoked, and two modes of the normal and PML grids can be switched by 1-bit flag, "normal/PML", each other. The dedicated circuit of Fig.2 executes the FDTD scheme to use grid information of PEC/vacuum flag, material constants, normal/PML flag which are downloaded from a

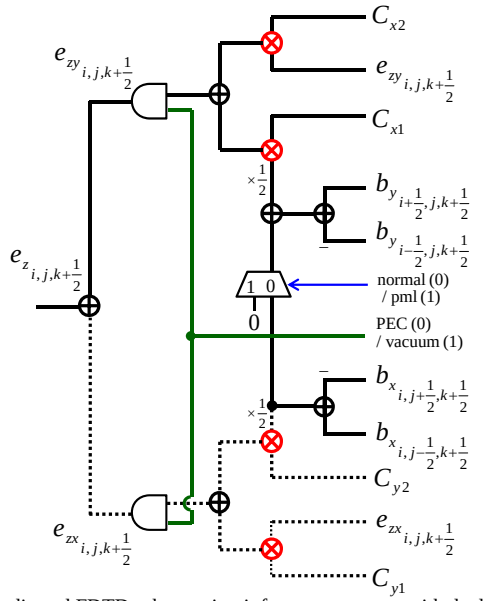

Fig. 2. Dedicated FDTD scheme circuit for e_z component with dual modes

host computer in advance of the simulation operation. Accordingly the FDTD dedicated circuit can treat various kinds of numerical models of any 3-D shapes, material distribution, PML grid allocation, by pre-setting these grid information without any modification of hardware circuits. Actually, it was shown that the dataflow FDTD machine operates normally by circuit simulations for a numerical example of 3-D rectangular waveguide [5].

III. Improved Circuit of FDTD Dataflow Machine

In the dedicated FDTD scheme circuit of the conventional dataflow machine (Fig.2), the most part of hardware circuit is occupied by four multiplexers. Then, only two multiplexers

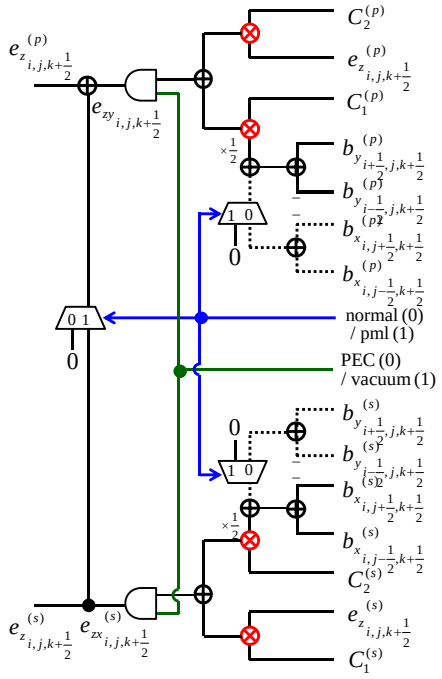

Fig. 3. Improved dedicated FDTD scheme circuit for e_z component

are used in the normal grid mode ("normal/PML"=0, full line part in Fig.2) and remaining two multiplexers are activated only in the PML grid mode ("normal/PML"=1), that is, almost a half amount of the hardware of the dedicated circuit is not used since the PML grids occupies only a few percent of entire grid space usually. To improve this inefficient use of hardware circuit of the conventional machine, this paper proposes the modified dedicated circuit indicated in Fig.3. The dedicated circuit of Fig.3 calculates the normal FDTD scheme for two grids in the normal grid mode or the PML scheme for a single grid in the PML grid mode. In this case, four multiplexers are always activated in both modes and only two adders are unused at the PML grids, which is a negligible amount. To apply this operation for 3-D simulations, the dedicated circuit of Fig.3 is extended to 2 x 2 x 2 grid region, which calculates 8 normal or 4 PML grids, indicated in Fig.4.

IV. Summary

This paper has presented a conceptual design of improved dataflow architecture of the 3-D FDTD method dedicated computer for the efficient implementation on the FPGA. It is estimated that two times larger grid space can be implemented in the single FPGA and two times higher performance is obtained in microwave simulations by this modifications compared with the conventional dataflow machine. The detail circuit design by the Hardware Description Language (HDL) is now being carried out, and will be presented with circuit simulations.

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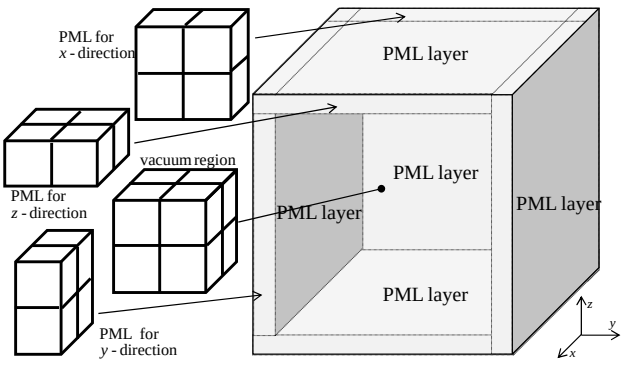

Fig. 4. 3-D configuration of improved dedicated FDTD scheme circuit